

IN THE CLAIMS:

Please amend the claims as follows.

1-5. (Canceled)

6. (Previously presented) An improved digital-data receiver synchronization apparatus comprising:

a plurality of memory devices for receiving multiple timing signals;

feedback means interconnecting said memory devices and cross-coupling signals produced by said memory devices; and

a common frequency reference source in communication with said plurality of memory devices for driving said plurality of memory devices,

wherein said multiple timing signals satisfy the relationship

$$f_1 = M \cdot f_2 = M \cdot N \cdot f_3$$

wherein  $f_1$  is said RF signal;  $f_2$  is said data bit rate signal;  $f_3$  is said data frame-rate signal; and  $M$  and  $N$  are positive rational numbers.

7. (Canceled)

8. (Previously presented) An improved digital-data receiver synchronization apparatus comprising:

a plurality of memory devices for receiving multiple timing signals;

feedback means interconnecting said memory devices and cross-coupling signals produced by said memory devices; and

a common frequency reference source in communication with said plurality of memory devices for driving said plurality of memory devices,  
wherein said common frequency reference uses edge-triggered synchronous logic.

9-14. (Canceled)

15. (Previously presented) An improved digital-data receiver synchronization apparatus comprising:

a plurality of memory devices for receiving multiple timing signals, at least one of said plurality of memory devices comprising a composite phase-frequency detector;

a common frequency reference source in communication with said plurality of memory devices for driving said plurality of memory devices; and,

a feedback means interconnecting said memory devices and for cross-coupling certain signals produced by said memory devices,

wherein said multiple timing signals satisfy the relationship:

$$f_1 = M f_2 = M N f_3$$

wherein  $f_1$  is said RF signal;  $f_2$  is said data bit-rate signal;  $f_3$  is said data frame-rate signal; and  $M$  and  $N$  are positive rational numbers.

16. (Previously presented) An improved digital-data receiver synchronization apparatus comprising:

a plurality of memory devices for receiving multiple timing signals, at least one of said plurality of memory devices comprising a composite phase-frequency detector;

a common frequency reference source in communication with said plurality of memory devices for driving said plurality of memory devices; and,

a feedback means interconnecting said memory devices and for cross-coupling certain signals produced by said memory devices,

wherein said common frequency reference uses edge-triggered synchronous logic.

17-18. (Cancelled)

19. (Previously presented) An improved digital-data receiver synchronization apparatus comprising:

a plurality of memory devices for receiving multiple timing signals, at least one of said plurality of memory devices comprising a composite phase-frequency detector;

a common frequency reference source in communication with said plurality of memory devices for driving said plurality of memory devices; and,

a feedback means interconnecting said memory devices and for cross-coupling certain signals produced by said memory devices,

wherein said composite phase-frequency detector further includes at least one device selected from the group consisting of a switch; a relay; a digital trigger (T) flip-flop; a digital divider; a nonlinear element; an analog divider; a square-root circuit; a comparator; a frequency-to-voltage converter; a frequency-to-current converter; a digital AND gate; a digital OR gate; a digital XOR gate; a digital counter; a digital J-K flip-flop; a digital R-S flip-flop; a majority-logic circuit; a peak detector; an average detector; a root-mean-square (RMS) detector; an operational amplifier; a follower circuit; a logic array device; a microprocessor; a digital state machine; a neural network; a digital signal processor (DSP) device; and an analog signal processor (ASP) device.

20. (Previously presented) An improved digital-data receiver synchronization apparatus comprising:

a plurality of memory devices for receiving multiple timing signals, at least one of said plurality of memory devices comprising a composite phase-frequency detector;

a common frequency reference source in communication with said plurality of memory devices for driving said plurality of memory devices; and,

a feedback means interconnecting said memory devices and for cross-coupling certain signals produced by said memory devices,

wherein said composite phase-frequency detector comprises a timing device for limiting the detector signal pulse widths.

21. (Previously presented) An improved digital-data receiver synchronization apparatus comprising:

a plurality of memory devices for receiving multiple timing signals, at least one of said plurality of memory devices comprising a composite phase-frequency detector;

a common frequency reference source in communication with said plurality of memory devices for driving said plurality of memory devices; and,

a feedback means interconnecting said memory devices and for cross-coupling certain signals produced by said memory devices,

wherein said composite phase-frequency detector further comprises at least one device selected from the group consisting of: a monostable multivibrator; a delay generator; a digital counter; a logic gate; a switch; a digital state machine; a pulse width-to-voltage converter; a pulse width-to-current converter; an integrator; a comparator; and a pulse width-limiting circuit.

22. (Previously presented) An improved digital-data receiver synchronization apparatus comprising:

a plurality of memory devices for receiving multiple timing signals, at least one of said plurality of memory devices comprising a composite phase-frequency detector;

a common frequency reference source in communication with said plurality of memory devices for driving said plurality of memory devices; and,

a feedback means interconnecting said memory devices and for cross-coupling certain signals produced by said memory devices,

wherein said composite phase-frequency detector further comprises an input-signal rate-limiting amplifier whereby said composite phase-frequency detector will not follow a signal having oscillations above a predetermined rate of change.

23. (Original) The improved digital-data receiver synchronization apparatus of claim 22, wherein said rate of change is measured in voltage (volts) per second.

24. (Original) The improved digital-data receiver synchronization apparatus of claim 22, wherein said rate of change is measured in current (amps) per second.

25-30. (Canceled)